Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 15 of 15 returned.

☐ 1. Document ID: US 6643737 B1

Using default format because multiple data bases are involved.

L7: Entry 1 of 15 File: USPT Nov 4, 2003

US-PAT-NO: 6643737
DOCUMENT-IDENTIFIER: US 6643737 B1

TITLE: Cache lock device and method therefor

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ono; Shinsuke	Tokyo			JP

US-CL-CURRENT: 711/128; 711/133, 711/136, 711/144, 711/145

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6618803 B1

L7: Entry 2 of 15 File: USPT Sep 9, 2003

US-PAT-NO: 6618803
DOCUMENT-IDENTIFIER: US 6618803 B1

TITLE: System and method for finding and validating the most recent advance load for a given checkload

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6216200 B1

L7: Entry 3 of 15 File: USPT Apr 10, 2001

US-PAT-NO: 6216200
DOCUMENT-IDENTIFIER: US 6216200 B1

TITLE: Address queue

h e b b g e e e f e h h ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6154812 A

L7: Entry 4 of 15 File: USPT Nov 28, 2000

US-PAT-NO: 6154812
DOCUMENT-IDENTIFIER: US 6154812 A

TITLE: Method for inhibiting thrashing in a multi-level non-blocking cache system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6148371 A

L7: Entry 5 of 15 File: USPT Nov 14, 2000

US-PAT-NO: 6148371
DOCUMENT-IDENTIFIER: US 6148371 A

TITLE: Multi-level non-blocking cache system with inhibiting thrashing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6081873 A

L7: Entry 6 of 15 File: USPT Jun 27, 2000

US-PAT-NO: 6081873
DOCUMENT-IDENTIFIER: US 6081873 A
**** See image for Certificate of Correction ****

TITLE: In-line bank conflict detection and resolution in a multi-ported non-blocking cache

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6041396 A

L7: Entry 7 of 15 File: USPT Mar 21, 2000

US-PAT-NO: 6041396
DOCUMENT-IDENTIFIER: US 6041396 A

TITLE: Segment descriptor cache addressed by part of the physical address of the desired descriptor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e h h ef b e

☐ 8. Document ID: US 6029212 A

L7: Entry 8 of 15 File: USPT Feb 22, 2000

US-PAT-NO: 6029212
DOCUMENT-IDENTIFIER: US 6029212 A

TITLE: Method of handling arbitrary size message queues in which a message is written into an aligned block of external registers within a plurality of external registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 9. Document ID: US 5930819 A

L7: Entry 9 of 15 File: USPT Jul 27, 1999

US-PAT-NO: 5930819
DOCUMENT-IDENTIFIER: US 5930819 A

TITLE: Method for performing in-line bank conflict detection and resolution in a multi-ported non-blocking cache

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 5845103 A

L7: Entry 10 of 15 File: USPT Dec 1, 1998

US-PAT-NO: 5845103
DOCUMENT-IDENTIFIER: US 5845103 A

TITLE: Computer with dynamic instruction reuse

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 11. Document ID: US 5835925 A

L7: Entry 11 of 15 File: USPT Nov 10, 1998

US-PAT-NO: 5835925
DOCUMENT-IDENTIFIER: US 5835925 A

TITLE: Using external registers to extend memory reference capabilities of a microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e h h ef b e

☐ 12. Document ID: US 5644748 A

L7: Entry 12 of 15 File: USPT Jul 1, 1997

US-PAT-NO: 5644748
DOCUMENT-IDENTIFIER: US 5644748 A
** See image for Certificate of Correction **

TITLE: Processor system including an index buffer circuit and a translation look-aside buffer control circuit for processor-to-processor interfacing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 13. Document ID: US 5621896 A

L7: Entry 13 of 15 File: USPT Apr 15, 1997

US-PAT-NO: 5621896
DOCUMENT-IDENTIFIER: US 5621896 A

TITLE: Data processor with unified store queue permitting hit under miss memory accesses

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 14. Document ID: US 5406504 A

L7: Entry 14 of 15 File: USPT Apr 11, 1995

US-PAT-NO: 5406504
DOCUMENT-IDENTIFIER: US 5406504 A

TITLE: Multiprocessor cache examiner and coherency checker

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 15. Document ID: US 5305458 A

L7: Entry 15 of 15 File: USPT Apr 19, 1994

US-PAT-NO: 5305458
DOCUMENT-IDENTIFIER: US 5305458 A

TITLE: Multiple virtual storage system and address control apparatus having a designation table holding device and translation buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

h e b b g e e e f e h h ef b e

Term	Documents
(3 AND 4).PGPB,USPT.	15
(L3 AND L4).PGPB,USPT.	15

Display Format: - Change Format

Previous Page Next Page Go to Doc#

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 20 of 69 returned.

☐ 1. Document ID: US 20030217251 A1

Using default format because multiple data bases are involved.

L14: Entry 1 of 69 File: PGPB Nov 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030217251
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030217251 A1

TITLE: Prediction of load-store dependencies in a processing agent

PUBLICATION-DATE: November 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Jourdan, Stephan J.	Portland	OR	US	
Boggs, Darrell D.	Aloha	OR	US	
Miller, John Alan	Portland	OR	US	
Singhal, Ronak	Beaverton	OR	US	

US-CL-CURRENT: 712/225; 712/216

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 2. Document ID: US 20030200402 A1

L14: Entry 2 of 69 File: PGPB Oct 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030200402
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030200402 A1

TITLE: Memory isolation through address translation data edit control

PUBLICATION-DATE: October 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Willman, Bryan Mark	Bellevue	WA	US	
England, Paul			US	
Peinado, Marcus			US	

h e b b g e e e f e f ef b e

US-CL-CURRENT: 711/154; 711/202

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 3. Document ID: US 20030177340 A1

L14: Entry 3 of 69 File: PGPB Sep 18, 2003

PGPUB-DOCUMENT-NUMBER: 20030177340
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030177340 A1

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

PUBLICATION-DATE: September 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Janik, Kenneth J.	Hillsboro	OR	US	
Lu, Shih-Lien L.	Corvallis	OR	US	
Miller, Michael F.	Hillsboro	OR	US	

US-CL-CURRENT: 712/219; 712/23

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 4. Document ID: US 20020174320 A1

L14: Entry 4 of 69 File: PGPB Nov 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020174320
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020174320 A1

TITLE: Index-based scoreboarding system and method

PUBLICATION-DATE: November 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yeluri, Sharada	San Jose	CA	US	

US-CL-CURRENT: 712/217

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 5. Document ID: US 20020099928 A1

L14: Entry 5 of 69 File: PGPB Jul 25, 2002

h e b b g e e e f e f ef b e

PGPUB-DOCUMENT-NUMBER: 20020099928
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020099928 A1

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

PUBLICATION-DATE: July 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Janik, Kenneth J.	Hillsboro	OR	US	
Lu, Shih-Lien L.	Corvallis	OR	US	
Miller, Michael F.	Hillsboro	OR	US	

US-CL-CURRENT: 712/216; 712/219

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 20010010073 A1

L14: Entry 6 of 69 File: PGPB Jul 26, 2001

PGPUB-DOCUMENT-NUMBER: 20010010073
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010010073 A1

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

PUBLICATION-DATE: July 26, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Janik, Kenneth J.	Hillsboro	OR	US	
Lu, Shih-Lien L.	Corvallis	OR	US	
Miller, Michael F.	Hillsboro	OR	US	

US-CL-CURRENT: 712/218

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 20010010072 A1

L14: Entry 7 of 69 File: PGPB Jul 26, 2001

PGPUB-DOCUMENT-NUMBER: 20010010072
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010010072 A1

TITLE: Instruction translator translating non-native instructions for a processor

h e b b g e e e f e f ef b e

into native instructions therefor, instruction memory with such translator, and data processing apparatus using them

PUBLICATION-DATE: July 26, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yoshida, Toyohiko	Hyogo		JP	

US-CL-CURRENT: 712/209; 712/210, 712/227

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6691222 B2

L14: Entry 8 of 69 File: USPT Feb 10, 2004

US-PAT-NO: 6691222
DOCUMENT-IDENTIFIER: US 6691222 B2

TITLE: Non-stalling circular counterflow pipeline processor with recorder buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6662280 B1

L14: Entry 9 of 69 File: USPT Dec 9, 2003

US-PAT-NO: 6662280
DOCUMENT-IDENTIFIER: US 6662280 B1

TITLE: Store buffer which forwards data based on index and optional way match

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 10. Document ID: US 6553485 B2

L14: Entry 10 of 69 File: USPT Apr 22, 2003

US-PAT-NO: 6553485
DOCUMENT-IDENTIFIER: US 6553485 B2

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 11. Document ID: US 6553482 B1

L14: Entry 11 of 69 File: USPT Apr 22, 2003

h e b b g e e e f e f ef b e

US-PAT-NO: 6553482
DOCUMENT-IDENTIFIER: US 6553482 B1

TITLE: Universal dependency vector/queue entry

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 12. Document ID: US 6505293 B1

L14: Entry 12 of 69 File: USPT Jan 7, 2003

US-PAT-NO: 6505293
DOCUMENT-IDENTIFIER: US 6505293 B1

TITLE: Register renaming to optimize identical register values

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 13. Document ID: US 6418525 B1

L14: Entry 13 of 69 File: USPT Jul 9, 2002

US-PAT-NO: 6418525
DOCUMENT-IDENTIFIER: US 6418525 B1

TITLE: Method and apparatus for reducing latency in set-associative caches using set prediction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 14. Document ID: US 6351805 B1

L14: Entry 14 of 69 File: USPT Feb 26, 2002

US-PAT-NO: 6351805
DOCUMENT-IDENTIFIER: US 6351805 B1
**** See image for Certificate of Correction ****

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 15. Document ID: US 6308259 B1

L14: Entry 15 of 69 File: USPT Oct 23, 2001

US-PAT-NO: 6308259
DOCUMENT-IDENTIFIER: US 6308259 B1
**** See image for Certificate of Correction ****

h e b b g e e e f e f ef b e

TITLE: Instruction queue evaluating dependency vector in portions during different clock phases

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 16. Document ID: US 6247115 B1

L14: Entry 16 of 69 File: USPT Jun 12, 2001

US-PAT-NO: 6247115
DOCUMENT-IDENTIFIER: US 6247115 B1
** See image for Certificate of Correction **

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 17. Document ID: US 6233244 B1

L14: Entry 17 of 69 File: USPT May 15, 2001

US-PAT-NO: 6233244
DOCUMENT-IDENTIFIER: US 6233244 B1

TITLE: Method and apparatus for reclaiming buffers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 18. Document ID: US 6216219 B1

L14: Entry 18 of 69 File: USPT Apr 10, 2001

US-PAT-NO: 6216219
DOCUMENT-IDENTIFIER: US 6216219 B1

TITLE: Microprocessor circuits, systems, and methods implementing a load target buffer with entries relating to prefetch desirability

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 19. Document ID: US 6216200 B1

L14: Entry 19 of 69 File: USPT Apr 10, 2001

US-PAT-NO: 6216200
DOCUMENT-IDENTIFIER: US 6216200 B1

TITLE: Address queue

h e b b g e e e f e f ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 20. Document ID: US 6212623 B1

L14: Entry 20 of 69 File: USPT Apr 3, 2001

US-PAT-NO: 6212623
DOCUMENT-IDENTIFIER: US 6212623 B1
** See image for Certificate of Correction **

TITLE: Universal dependency vector/queue entry

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
LOAD	1649126
LOADS	384934
POINT$3	0
POINT	3755064
POINTA	394
POINTAB	3
POINTABO	1
POINTAB6	1
POINTAC	1
POINTACL	3
POINTAC3	1
(L11 AND LOAD NEAR5 (POINT$3 OR INDEX$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	69

There are more results than shown above. Click here to view the entire set.

Display Format: - Change Format

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h e b b g e e e f e f ef b e

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 40 of 69 returned.

☐ 21. Document ID: US 6212622 B1

Using default format because multiple data bases are involved.

L14: Entry 21 of 69 File: USPT Apr 3, 2001

US-PAT-NO: 6212622
DOCUMENT-IDENTIFIER: US 6212622 B1

TITLE: Mechanism for load block on store address generation

DATE-ISSUED: April 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Witt; David B.	Austin	TX		

US-CL-CURRENT: 712/216; 712/2, 712/234, 712/239, 712/5, 712/7

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 22. Document ID: US 6163839 A

L14: Entry 22 of 69 File: USPT Dec 19, 2000

US-PAT-NO: 6163839
DOCUMENT-IDENTIFIER: US 6163839 A
** See image for Certificate of Correction **

TITLE: Non-stalling circular counterflow pipeline processor with reorder buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 23. Document ID: US 6122727 A

L14: Entry 23 of 69 File: USPT Sep 19, 2000

US-PAT-NO: 6122727
DOCUMENT-IDENTIFIER: US 6122727 A

TITLE: Symmetrical instructions queue for high clock frequency scheduling

h e b b cg b cc e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 24. Document ID: US 6108770 A

L14: Entry 24 of 69 File: USPT Aug 22, 2000

US-PAT-NO: 6108770
DOCUMENT-IDENTIFIER: US 6108770 A

TITLE: Method and apparatus for predicting memory dependence using store sets

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 25. Document ID: US 6098167 A

L14: Entry 25 of 69 File: USPT Aug 1, 2000

US-PAT-NO: 6098167
DOCUMENT-IDENTIFIER: US 6098167 A

TITLE: Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 26. Document ID: US 6061777 A

L14: Entry 26 of 69 File: USPT May 9, 2000

US-PAT-NO: 6061777
DOCUMENT-IDENTIFIER: US 6061777 A

TITLE: Apparatus and method for reducing the number of rename registers required in the operation of a processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 27. Document ID: US 6047369 A

L14: Entry 27 of 69 File: USPT Apr 4, 2000

US-PAT-NO: 6047369
DOCUMENT-IDENTIFIER: US 6047369 A

TITLE: Flag renaming and flag masks within register alias table

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b cg b cc e

☐ 28. Document ID: US 6026485 A

L14: Entry 28 of 69 File: USPT Feb 15, 2000

US-PAT-NO: 6026485
DOCUMENT-IDENTIFIER: US 6026485 A

TITLE: Instruction folding for a stack-based machine

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 29. Document ID: US 6016542 A

L14: Entry 29 of 69 File: USPT Jan 18, 2000

US-PAT-NO: 6016542
DOCUMENT-IDENTIFIER: US 6016542 A

TITLE: Detecting long latency pipeline stalls for thread switching

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 30. Document ID: US 5974524 A

L14: Entry 30 of 69 File: USPT Oct 26, 1999

US-PAT-NO: 5974524
DOCUMENT-IDENTIFIER: US 5974524 A

TITLE: Method and apparatus for reducing the number of rename registers in a processor supporting out-of-order execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 31. Document ID: US 5963984 A

L14: Entry 31 of 69 File: USPT Oct 5, 1999

US-PAT-NO: 5963984
DOCUMENT-IDENTIFIER: US 5963984 A

TITLE: Address translation unit employing programmable page size

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 32. Document ID: US 5961636 A

L14: Entry 32 of 69 File: USPT Oct 5, 1999

US-PAT-NO: 5961636

h e b b cg b cc e

DOCUMENT-IDENTIFIER: US 5961636 A

TITLE: Checkpoint table for selective instruction flushing in a speculative execution unit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 33. Document ID: US 5953512 A

L14: Entry 33 of 69 File: USPT Sep 14, 1999

US-PAT-NO: 5953512
DOCUMENT-IDENTIFIER: US 5953512 A

TITLE: Microprocessor circuits, systems, and methods implementing a loop and/or stride predicting load target buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 34. Document ID: US 5913048 A

L14: Entry 34 of 69 File: USPT Jun 15, 1999

US-PAT-NO: 5913048
DOCUMENT-IDENTIFIER: US 5913048 A

TITLE: Dispatching instructions in a processor supporting out-of-order execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 35. Document ID: US 5903749 A

L14: Entry 35 of 69 File: USPT May 11, 1999

US-PAT-NO: 5903749
DOCUMENT-IDENTIFIER: US 5903749 A

TITLE: Method and apparatus for implementing check instructions that allow for the reuse of memory conflict information if no memory conflict occurs

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 36. Document ID: US 5887161 A

L14: Entry 36 of 69 File: USPT Mar 23, 1999

US-PAT-NO: 5887161
DOCUMENT-IDENTIFIER: US 5887161 A

TITLE: Issuing instructions in a processor supporting out-of-order execution

h e b b cg b cc e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 37. Document ID: US 5875326 A

L14: Entry 37 of 69 File: USPT Feb 23, 1999

US-PAT-NO: 5875326
DOCUMENT-IDENTIFIER: US 5875326 A

TITLE: Data processing system and method for completing out-of-order instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 38. Document ID: US 5835745 A

L14: Entry 38 of 69 File: USPT Nov 10, 1998

US-PAT-NO: 5835745
DOCUMENT-IDENTIFIER: US 5835745 A

TITLE: Hardware instruction scheduler for short execution unit latencies

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 39. Document ID: US 5828874 A

L14: Entry 39 of 69 File: USPT Oct 27, 1998

US-PAT-NO: 5828874
DOCUMENT-IDENTIFIER: US 5828874 A

TITLE: Past-history filtered branch prediction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 40. Document ID: US 5826094 A

L14: Entry 40 of 69 File: USPT Oct 20, 1998

US-PAT-NO: 5826094
DOCUMENT-IDENTIFIER: US 5826094 A

TITLE: Register alias table update to indicate architecturally visible state

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

h e b b cg b cc e

Term	Documents
LOAD	1649126
LOADS	384934
POINT$3	0
POINT	3755064
POINTA	394
POINTAB	3
POINTABO	1
POINTAB6	1
POINTAC	1
POINTACL	3
POINTAC3	1
(L11 AND LOAD NEAR5 (POINT$3 OR INDEX$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	69

There are more results than shown above. Click here to view the entire set.

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h e b b cg b cc e

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 41 through 60 of 69 returned.

☐ 41. Document ID: US 5765206 A

Using default format because multiple data bases are involved.

L14: Entry 41 of 69 File: USPT Jun 9, 1998

US-PAT-NO: 5765206
DOCUMENT-IDENTIFIER: US 5765206 A

TITLE: System and method for emulating a segmented virtual address space by a microprocessor that provides a non-segmented virtual address space

DATE-ISSUED: June 9, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hohensee; Paul H.	Nashua	NH		
Dice; David	Foxboro	MA		
Vandette; Robert G.	Andover	MA		
Reese; David L.	Westborough	MA		

US-CL-CURRENT: 711/203

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 42. Document ID: US 5752274 A

L14: Entry 42 of 69 File: USPT May 12, 1998

US-PAT-NO: 5752274
DOCUMENT-IDENTIFIER: US 5752274 A

TITLE: Address translation unit employing a victim TLB

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 43. Document ID: US 5727176 A

L14: Entry 43 of 69 File: USPT Mar 10, 1998

US-PAT-NO: 5727176

h e b b cg b cc e

DOCUMENT-IDENTIFIER: US 5727176 A
** See image for Certificate of Correction **

TITLE: Data processor with circuitry for handling pointers associated with a register exchange operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 44. Document ID: US 5715427 A

L14: Entry 44 of 69 File: USPT Feb 3, 1998

US-PAT-NO: 5715427
DOCUMENT-IDENTIFIER: US 5715427 A

TITLE: Semi-associative cache with MRU/LRU replacement

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 45. Document ID: US 5655096 A

L14: Entry 45 of 69 File: USPT Aug 5, 1997

US-PAT-NO: 5655096
DOCUMENT-IDENTIFIER: US 5655096 A

TITLE: Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 46. Document ID: US 5634119 A

L14: Entry 46 of 69 File: USPT May 27, 1997

US-PAT-NO: 5634119
DOCUMENT-IDENTIFIER: US 5634119 A

TITLE: Computer processing unit employing a separate millicode branch history table

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 47. Document ID: US 5619662 A

L14: Entry 47 of 69 File: USPT Apr 8, 1997

US-PAT-NO: 5619662
DOCUMENT-IDENTIFIER: US 5619662 A

h e b b cg b cc e

TITLE: Memory reference tagging

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 48. Document ID: US 5613132 A

L14: Entry 48 of 69 File: USPT Mar 18, 1997

US-PAT-NO: 5613132
DOCUMENT-IDENTIFIER: US 5613132 A
** See image for Certificate of Correction **

TITLE: Integer and floating point register alias table within processor device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 49. Document ID: US 5581719 A

L14: Entry 49 of 69 File: USPT Dec 3, 1996

US-PAT-NO: 5581719
DOCUMENT-IDENTIFIER: US 5581719 A

TITLE: Multiple block line prediction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 50. Document ID: US 5564118 A

L14: Entry 50 of 69 File: USPT Oct 8, 1996

US-PAT-NO: 5564118
DOCUMENT-IDENTIFIER: US 5564118 A

TITLE: Past-history filtered branch prediction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 51. Document ID: US 5548776 A

L14: Entry 51 of 69 File: USPT Aug 20, 1996

US-PAT-NO: 5548776
DOCUMENT-IDENTIFIER: US 5548776 A
** See image for Certificate of Correction **

TITLE: N-wide bypass for data dependencies within register alias table

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b cg b cc e

☐ 52. Document ID: US 5524262 A

L14: Entry 52 of 69 File: USPT Jun 4, 1996

US-PAT-NO: 5524262
DOCUMENT-IDENTIFIER: US 5524262 A
** See image for Certificate of Correction **

TITLE: Apparatus and method for renaming registers in a processor and resolving data dependencies thereof

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 53. Document ID: US 5519841 A

L14: Entry 53 of 69 File: USPT May 21, 1996

US-PAT-NO: 5519841
DOCUMENT-IDENTIFIER: US 5519841 A

TITLE: Multi instruction register mapper

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 54. Document ID: US 5499352 A

L14: Entry 54 of 69 File: USPT Mar 12, 1996

US-PAT-NO: 5499352
DOCUMENT-IDENTIFIER: US 5499352 A
** See image for Certificate of Correction **

TITLE: Floating point register alias table FXCH and retirement floating point register array

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 55. Document ID: US 5471633 A

L14: Entry 55 of 69 File: USPT Nov 28, 1995

US-PAT-NO: 5471633
DOCUMENT-IDENTIFIER: US 5471633 A

TITLE: Idiom recognizer within a register alias table

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b cg b cc e

☐ 56. Document ID: US 5471593 A

L14: Entry 56 of 69 File: USPT Nov 28, 1995

US-PAT-NO: 5471593
DOCUMENT-IDENTIFIER: US 5471593 A

TITLE: Computer processor with an efficient means of executing many instructions simultaneously

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 57. Document ID: US 5446912 A

L14: Entry 57 of 69 File: USPT Aug 29, 1995

US-PAT-NO: 5446912
DOCUMENT-IDENTIFIER: US 5446912 A
** See image for Certificate of Correction **

TITLE: Partial width stalls within register alias table

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 58. Document ID: US 4890223 A

L14: Entry 58 of 69 File: USPT Dec 26, 1989

US-PAT-NO: 4890223
DOCUMENT-IDENTIFIER: US 4890223 A
** See image for Certificate of Correction **

TITLE: Paged memory management unit which evaluates access permissions when creating translator

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 59. Document ID: US 4860197 A

L14: Entry 59 of 69 File: USPT Aug 22, 1989

US-PAT-NO: 4860197
DOCUMENT-IDENTIFIER: US 4860197 A

TITLE: Branch cache system with instruction boundary determination independent of parcel boundary

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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h e b b cg b cc e

☐ 60. Document ID: US 4800489 A

L14: Entry 60 of 69 File: USPT Jan 24, 1989

US-PAT-NO: 4800489
DOCUMENT-IDENTIFIER: US 4800489 A

TITLE: Paged memory management unit capable of selectively supporting multiple address spaces

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
LOAD	1649126
LOADS	384934
POINT$3	0
POINT	3755064
POINTA	394
POINTAB	3
POINTABO	1
POINTAB6	1
POINTAC	1
POINTACL	3
POINTAC3	1
(L11 AND LOAD NEAR5 (POINT$3 OR INDEX$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	69

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Term	Documents
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LOADS	384934
POINT$3	0
POINT	3755064
POINTA	394
POINTAB	3
POINTABO	1
POINTAB6	1
POINTAC	1
POINTACL	3
POINTAC3	1
(L11 AND LOAD NEAR5 (POINT$3 OR INDEX$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	69

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Search History

DATE: Wednesday, March 03, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set

h e b b cg b e e ch

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L14	L11 and load near5 (point$3 or index$3)	69	L14
L13	L11 and load near8 (point$3 or index$3)	80	L13
L12	L11 and load	139	L12
L11	L10 and l8	167	L11
L10	L4 and (scoreboard$3 or table$1 or cache) near6 entr$3 near8 associat$5	215	L10
L9	L8 and l7	400	L9
L8	l2 or l3	22743	L8
L7	L6 and associat$4	565	L7
L6	L4 and (scoreboard$3 or table$1 or array or cache) near6 entr$3	581	L6
L5	L4 and (scoreboard$3 or table$1 or array)	659	L5
L4	l1 and (valid$6 or invalid$6) near5 entr$3	724	L4

DB=PGPB,USPT; PLUR=YES; OP=OR

L3	(712/26-248)![CCLS]	8133	L3
L2	(711/117-221)![CCLS]	15723	L2

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L1	(index$3 or point$3) near7 entr$3 near8 (load or instruction$1)	2723	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Three extensions to register integration

Petric, V. Bracy, A. Roth, A.
Dept. of Comput. & Inf. Sci., Pennsylvania Univ., Philadelphia, PA, USA

This paper appears in: **Microarchitecture, 2002. (MICRO-35). Proceedin Annual IEEE/ACM International Symposium on**

Publication Date: 18-22 Nov. 2002
On page(s): 37 - 47
ISSN: 1072-4451
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Inspec Accession Number: 7568999

Abstract:
Register integration (or just integration) is a register renaming discipline that implements instruction reuse via physical register sharing. Initially developec squash reuse, the integration mechanism can exploit more reuse scenarios. H describe three extensions to the original design that expand its applicability a performance impact. First, we extend squash reuse to general reuse. Wherea reuse maintains the concept of an instruction instance "owning" its output re allow multiple instructions to simultaneously share a single register. Next, we PC-**indexing** scheme with an opcode-based **indexing** scheme that exposes r integration opportunities. Finally, we introduce an extension called reverse in which we speculatively create integration **entries** for the inverses of operatio instance, when renaming an add, we create an **entry** for the inverse subtract integration allows us to reuse operations that the program itself has not exec We use reverse integration to implement speculative memory bypassing for stack-pointer based **loads** (register fills and restores). Our evaluation shows extensions increase the integration rate - the number of retired instructions t integrate older results and bypass the execution engine -to an average of 15 SPEC2000 integer benchmarks. On a 4-way superscalar processor with an ag memory system, this translates into an average IPC improvement of 7%. The integrating instructions completely bypass the execution engine raises the po using integration as a low-complexity substitute for execution bandwidth and buffering. Our experiments show that such a trade-off is possible, enabling a IPC/complexity designs.

Index Terms:
computer architecture performance evaluation instruction reuse register fills registe

register renaming register sharing restores speculative memory bypassing squash stack-pointer based loads

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